Leakage Power Optimization by Sleepy Keeper Gate Replacement Techniques

*Ms. Rupali Asati (Pursuing M.Tech (VLSI Design)),
**Prof. Neeraj Singh, SSSIST, Sehore (M.P.).

Abstract:
Power dissipation becoming a limiting factor in VLSI circuits and systems. Due to relatively high complexity of VLSI systems used in various applications, the power dissipation in CMOS inverter, arises from it's switching activity, which is mainly influenced by the supply voltage and effective capacitance. One of challenge with technology scaling is the rapid increase in sub threshold leakage power due to Vt reduction. Leakage power dissipation is a component of static power dissipation in CMOS circuits. It is caused by the presence of leakage currents in the MOS transistors. Leakage power can be reduce by Stack, Sleep and Sleepy keeper transistor techniques. Sleepy Keeper technique provided lesser static power dissipation and lesser static power delay product in comparison with the other techniques. The main advantage of using Sleepy Keeper technique is that it retains the logic state and also lowers the sub threshold leakage power dissipation. It has been shown previously that the stacking of two off transistors has significantly reduced sub-threshold leakage compared to a single off transistor.

1. Leakage Power Source:

Sub threshold leakage current is the most dominant component of leakage current (power) in short channel MOS transistors. This leakage current is caused by the inability to completely turn off a MOS transistor. Due to the reversely biased PN junction the transistor conducts even in weak inversion region below the threshold voltage of the MOS transistor.

There are four main sources of leakage current in a CMOS transistor

1. Junction Leakage(I1): The junction leakage occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is OFF. A reverse-biased PN junction leakage has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction.

2. Gate-Induced Drain Leakage(I3): The gate induced drain leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor with grounded gate and drain potential at VDD, significant band bending in the drain allows electron-hole pair generation through avalanche multiplication and band-to-band tunnelling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are collected by the drain, resulting in GIDL current.

3. Gate Direct Tunnelling Leakage(I2): This current results from the tunnelling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer. This direct tunnelling

current increases exponentially with the gate oxide thickness and supply voltage.

4. Sub threshold Leakage(I4): The sub threshold leakage is the drain-source current of a transistor I.e channel punch through current.

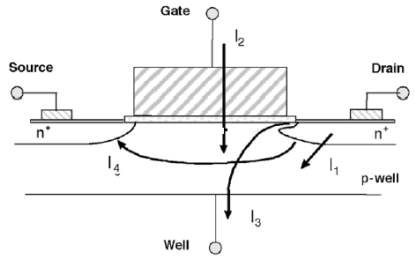

Fig 1 Leakage currents in MOSFET

Increasing the threshold voltage of a transistor reduces the leakage current exponentially, but it has a marginal effect on the dynamic power dissipation. On the other hand, reducing the width of a transistor reduces both leakage and dynamic power, but at a linear rate only.

2. Stack technique

In this technique NMOS and PMOS transistors can be added in series with gates to increase the stack effect, it will increase the resistance between the supply and ground. Therefore, the leakage of the logic gate is reduced. A MOS transistor in the circuit is divided and stacked into two half width size transistors. When two half size stacked MOS transistors are turned off together, induce reverse bias between them results in the reduction of the sub threshold leakage power . However, increase in the number of transistors increases the overall propagation delay of the circuit. When a stack of two or more transistors are turned off, the time required for voltages and currents to settle to quiescent levels is large and can vary over a wide range.

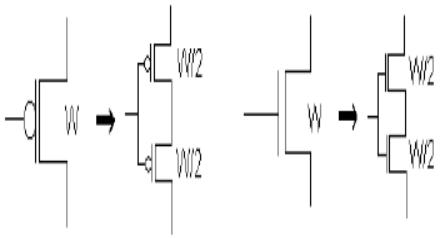

Fig 2 Stack Technique series connected half channel width MOSFET.

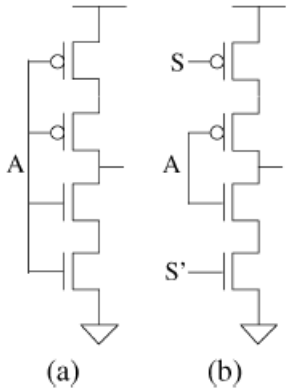

Fig Not logic Gate using (a)stack method (b) Sleep transistor method.

3. Sleep Technique

Sleep transistors of high threshold voltages are used in the Sleep technique. A sleep PMOS transistor is placed between the supply voltage, VDD and the pull-up network and a sleep NMOS transistor is placed between the pull down network and the ground, GND. These sleep transistors are turned ON when the circuit is in active state and turned OFF when the circuit is in sleep state. This technique reduces the sub threshold leakage current by cutting off the logic circuitry from the power supply voltage and ground in the sleep state. These sleep transistors are driven by sleep signals. Using this technique the present state of the circuit is lost and thus results in destruction of the present logic state.

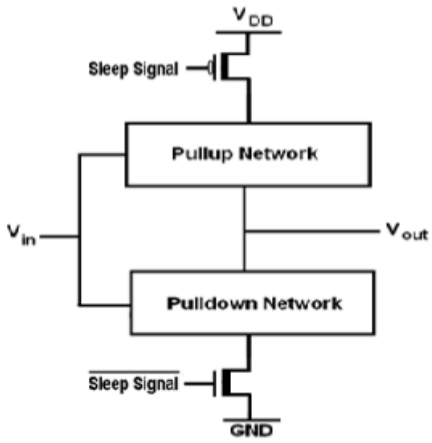

Fig 3 Sleep transistor technique

4. Sleepy Keeper Technique:

In this technique, an additional high threshold voltage NMOS transistor is connected in parallel with the sleep PMOS transistor and an additional high threshold voltage PMOS transistor is connected in parallel with the sleep NMOS transistor. In sleep mode, the sleep transistors are in cut-off state. So, when sleep signal is activated, then the high threshold voltage NMOS transistor connected in parallel

with the sleep PMOS transistor is the only source of power supply to the pull-up network and the high threshold voltage PMOS transistor connected in parallel with the sleep NMOS transistor provides the path to connect the pull down network with ground. The major advantage in using Sleepy keeper technique is that it reduces the significant sub threshold leakage current and also retains the circuit present state in sleep mode.

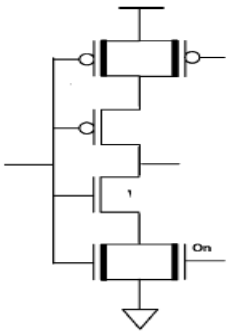

Fig 4. Sleepy Transistor technique.

3. Our design :

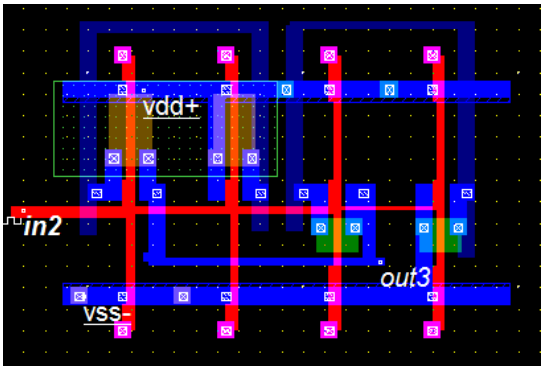

Fig Layout design of Not ate using Stack method

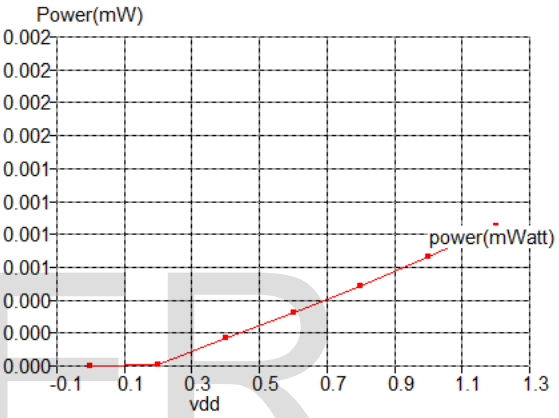

Fig Power dissipation of Not ate using Stack method

In stack transistor technique two half channel width transistors are connected in series to for one of the transistor in pull up and pull down networks with gates to increase the stack effect, it will increase the resistance between the supply and ground. Therefore, the leakage of the logic gate is reduced. A MOS transistor in the circuit is divided and stacked into two half width size transistors. When two half size stacked MOS transistors are turned off together, induce reverse bias between them results in the reduction of the sub threshold leakage power . However, increase in the number of transistors increases the overall propagation delay of the circuit.

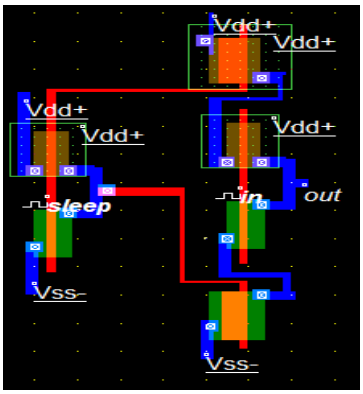

Fig Layout design of Not ate using sleep transistor method

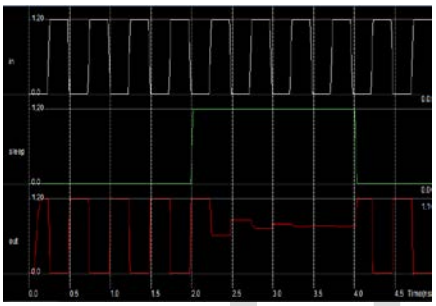

Fig Simulation wave of Not ate using sleep transistor method

Multi threshold voltage CMOS (MTCMOS) reduces the leakage by inserting high-threshold devices in series to low circuitry. A sleep control scheme is introduced for efficient power management. In the active mode, sleep signal is set low and sleep transistors are turned on. Since their on-resistances are small, the virtual supply voltages unction as real power lines. In the standby mode, sleep signal is set high, sleep transistors are turned off, and the leakage current is low.

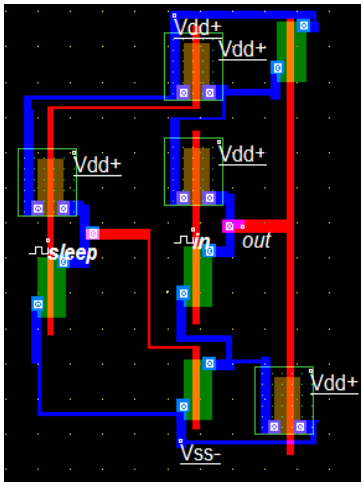

Fig Layout design of Not gate using Sleepy keeper method

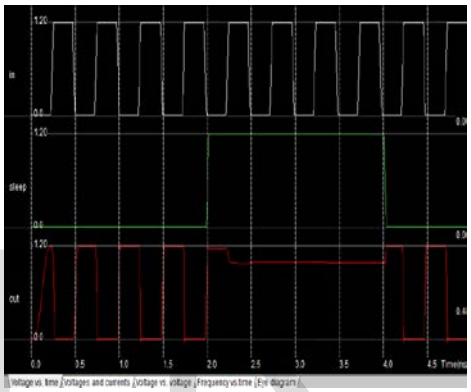

Fig Simulation wave of Not gate using Sleepy keeper method

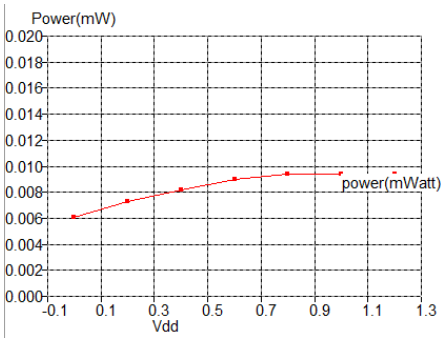

Fig Power dissipation of Not gate using Sleepy keeper method

The sleepy stack technique has a combined structure of the stack technique and the sleep transistor technique. However, unlike the sleep transistor technique, the sleepy stack technique retains exact logic state when in sleep mode; furthermore, unlike the forced stack technique, the sleepy stack technique

can utilize high threshold voltage transistors. the sleepy stack technique can achieve ultra-low leakage power consumption while saving state.

Conclusion:

Leakage power can be reduce by Stack, Sleep and Sleepy keeper transistor techniques. sleepy stack can achieve ultra-low leakage power consumption logic state during sleep mode . We apply the sleepy stack to generic logic circuits. Due to the robust nature of static CMOS logic, circuits in this technology family can operate with supply voltages below the transistor threshold voltage. Sleepy Keeper technique provided lesser static power dissipation and lesser static power delay product in comparison with the other techniques. The main advantage of using Sleepy Keeper technique is that it retains the logic state and also lowers the subthreshold leakage power dissipation.

References:

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